AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of detecting and relieving timing-based congestion during physical implementation of an integrated circuit, said method comprising:

routing connections of a circuit design for the integrated circuit in a delay mode, wherein the routed circuit design includes at least one instance of connection sharing;

calculating an initial delay for the connections of the circuit design;

predicting a final delay for the connections of the circuit design with [[were]] connection sharing ~~has been~~ removed, wherein the final delays are predicted according to the initial delays and a measure of connection sharing within the circuit design;

identifying connections of the circuit design that do not conform with timing constraints based upon at least one of the initial delays [[and]] or the final delays; and

selectively performing a detailed routing of the circuit design or further optimizing the identified connections of the circuit design according to said identifying step.

2. (Original) The method of claim 1, for each connection, said predicting step comprising:

determining a number of connections sharing each wire by said routing step;

summing the number of connections for each wire; and

adding the initial delay to a product of the summed number of connections and the initial delay.

3. (Original) The method of claim 2, said summing step comprising multiplying the summed number of connections by a weighting factor.

4. (Original) The method of claim 2, said step of adding the initial delay comprising first multiplying the product by a weighting factor.

5. (Original) The method of claim 1, said predicting step further comprising using a quadratic model to predict the final delays.

6. (Original) The method of claim 1, said step of further optimizing the circuit design comprising at least one of incrementally placing the circuit design or performing physical synthesis on the circuit design.

7. (Original) The method of claim 6, said step of further optimizing the circuit design comprising rerouting connections changed by said incrementally placing step.

8. (Currently Amended) A computer automated system for detecting and relieving timing-based congestion during physical implementation of an integrated circuit, said system comprising:

means for routing a placed circuit design for the integrated circuit in a delay mode, wherein the routed circuit design includes at least one instance of connection sharing;

means for calculating an initial delay for connections of the circuit design based upon said routing step;

means for predicting a final delay for the connections of the circuit design with [[were]] connection sharing ~~overlaps to be~~ removed, wherein the final delays are predicted according to the initial delays and connection sharing within the circuit design;

means for identifying connections of the circuit design that do not conform with timing constraints based upon at least one of the initial delays or the [[and]] final delays; and

means for selectively performing a detailed routing of the circuit design or further optimizing the identified connections of the circuit design according to a result obtained by said means for identifying.

9. (Original) The system of claim 8, said means for predicting comprising:

means for determining a number of connections assigned to each wire by said

means for routing;

means for summing the number of connections for each wire; and

means for adding the initial delay to a product of the summed number of connections and the initial delay.

10. (Original) The system of claim 9, said means for summing comprising means for multiplying the summed number of connections by a weighting factor.

11. (Original) The system of claim 9, said means for adding the initial delay comprising means for first multiplying the product by a weighting factor.

12. (Original) The system of claim 8, said means for predicting further comprising using a quadratic model to predict the final delays.

13. (Original) The system of claim 8, said means for selecting comprising at least one of means for incrementally placing the circuit design or performing physical synthesis on the circuit design.

14. (Original) The system of claim 13, said means for selecting comprising means for rerouting connections changed by said incrementally placing step.

15. (Currently Amended) A machine readable storage, having stored thereon a computer program having a plurality of code sections executable by a machine for causing the machine to perform the steps of:

routing a placed circuit design for an integrated circuit in a delay mode, wherein the routed circuit design includes at least one instance of connection sharing;

calculating an initial delay for connections of the circuit design based upon said routing step;

predicting a final delay for the connections of the circuit design with [[were]] connection sharing ~~overlaps to be~~ removed, wherein the final delays are predicted according to the initial delays and connection sharing within the circuit design;

identifying connections of the circuit design that do not conform with timing constraints based upon at least one of the initial delays or the [[and]] final delays; and

selectively performing a detailed routing of the circuit design or further optimizing the identified connections of the circuit design according to said identifying step.

16. (Original) The machine readable storage of claim 15, for each connection, said predicting step comprising:

determining a number of connections assigned to each wire by said routing step;

summing the number of connections for each wire; and

adding the initial delay to a product of the summed number of connections and the initial delay.

17. (Original) The machine readable storage of claim 16, said summing step comprising multiplying the summed number of connections by a weighting factor.

18. (Original) The machine readable storage of claim 16, said step of adding the initial delay comprising first multiplying the product by a weighting factor.

19. (Original) The method of claim 15, said predicting step further comprising using a quadratic model to predict the final delays.

20. (Original) The machine readable storage of claim 15, said step of further optimizing the circuit design comprising at least one of incrementally placing the circuit design or performing physical synthesis on the circuit design.

21. (Original) The machine readable storage of claim 20, said step of further optimizing the circuit design comprising rerouting connections changed by said incrementally placing step.